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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BROWN, JAYME L	

ART UNIT	PAPER NUMBER
1733	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,705	SANGIORGI, JAMES A.	
	Examiner	Art Unit	
	Jayme L. Brown	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/4/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1 and 9 contain new matter regarding the non-conductive bonding material around "only the edge of an area". There is no support in the original Specification for these added limitations.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 9, it is unclear as to where the edge of an area is. It is not defined in the Specification as to what the edge is.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Yagi et al. (U.S. Patent 6,651,320).

Regarding claim 1, Yagi et al. discloses a method for attaching a circuit element (103) to a substrate (101), comprising: applying a conductive bonding material (106) to a conductive portion (104) of at least one of the circuit element and the substrate; positioning the circuit element in a desired location on the substrate; heating the conductive bonding material to promote one or more conductive bonds; and applying a non-conductive bonding material (107, 161) around an area where the circuit element overlies the substrate to form a non-conductive bond between the circuit element and the substrate (Figures 4 and 20; Column 5, lines 46-60).

Applicant added the new limitation of the non-conductive bonding material being applied around only the edge of an area where the element overlies the substrate. Yagi et al. teaches this limitation in Figures 4 and 14.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Sakemi (U.S. Patent 5,817,542).

Regarding claim 1, Sakemi discloses a method for attaching a circuit element (5) to a substrate (1), comprising: applying a conductive bonding material (9) to a conductive portion (2 and 3) of at least one of the circuit element and the substrate; positioning the circuit element in a desired location on the substrate; heating the conductive bonding material to promote one or more conductive bonds; and applying a non-conductive bonding material (12) around an area where the circuit element overlies the substrate to form a non-conductive bond between the circuit element and the substrate (Figures 1C and 2C; Column 2, line 37 – Column 3, line 20).

Applicant adds the new limitation of the non-conductive bonding material being applied around only the edge of an area where the element overlies the substrate. Sakemi teaches this limitation in Figure 1C.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of American Technical Ceramics bulletin.

Regarding claim 2, Sakemi is relied upon for the teachings above. Sakemi is silent toward the conductive bonding material being an epoxy resin.

The American Technical Ceramics bulletin is directed toward techniques for attaching capacitors to substrates (printed circuit boards), such as soldering, conductive epoxy bonding, and wire bonding. The bulletin teaches that the conductive adhesive is an epoxy (Section 12.0).

One skilled in the art would have readily appreciated using a conductive epoxy as the conductive bonding material, since it is a conventional material to use when bonding circuit elements to circuit boards; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a conductive epoxy as the conductive bonding material in the method of Sakemi, as suggested by the American Technical Ceramics bulletin.

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of American Technical Ceramics bulletin and Lane et al. (U.S. Patent 6,599,619).

Regarding claim 6, Sakemi and the American Technical Ceramics bulletin are relied upon for the teachings above. Sakemi is silent toward the substrate comprising a laminate substrate and the conductive bonding material being an epoxy resin.

The limitations for the conductive bonding material comprising an epoxy resin are addressed above in claim 2.

Lane et al. is directed toward methods for producing electrical laminates from certain thermosetting resin compositions. Lane et al. teaches that electrical laminates such as circuit boards are produced by laminating sheets of electrical conducting material onto a base substrate of insulation material (Column 1, lines 15-17 and 24-28).

One skilled in the art would have readily appreciated using a laminated substrate, such as a circuit board, since it is a conventional substrate to use when attaching circuit elements; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a laminate substrate in the method of Sakemi, as modified above in claim 2, as suggested by Lane et al.

Regarding claim 7, Sakemi and the American Technical Ceramics bulletin are relied upon for the teachings above. Sakemi is silent toward the substrate comprising a laminate substrate and the conductive bonding material being a conductive solder.

The American Technical Ceramics bulletin teaches that a soldering is another technique for attaching a capacitor to a printed circuit board. A variety of solder compositions are available to suit specific application requirements, including ones that contain silver (Ag). Also, solder pastes or "creams" are frequently used. The American Technical Ceramics bulletin teaches that the conductive bonding material comprises of a conductive solder (Section 4.0; Table 1).

Lane et al. is directed toward methods for producing electrical laminates from certain thermosetting resin compositions. Lane et al. teaches that electrical laminates such as circuit boards are produced by laminating sheets of electrical conducting material onto a base substrate of insulation material (Column 1, lines 15-17 and 24-28).

One skilled in the art would have readily appreciated that a conductive solder is another conventional option for bonding circuit elements to a substrate. Also, one skilled in the art would have readily appreciated using a laminated substrate, such as a circuit board, since it is a conventional substrate to use when attaching circuit elements; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a laminate substrate and a conductive solder in the method of Sakemi, as suggested by Lane et al. and the American Technical Ceramics bulletin.

11. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of Ono et al. (U.S. Patent 6,890,789).

Regarding claim 3, Sakemi is relied upon for the teachings above. Sakemi is silent toward the non-conductive bonding material comprising a liquid underfill encapsulant material.

Ono et al. is directed to mounting a photo-semiconductor device (A), which is formed on a compound semiconductor substrate (B), flip-chip-wise on a circuit board (7). Electrode 3 of the photo-semiconductor device A is fixed onto the connection electrode 6 of the circuit board 7 via a conductive adhesive agent 4. The connection between the photo-semiconductor device and the circuit board is encapsulated and reinforced by an encapsulating resin 5 (flip-chip underfill material) (Figure 1; Column 4, line 58 – Column 5, line 17). Ono et al. teaches that the non-conductive bonding material comprises a liquid underfill encapsulant material (flip-chip underfill material) (Figure 8C; Column 10, lines 29-33).

One skilled in the art would have readily appreciated that the non-conductive bonding material be a liquid underfill encapsulant material (flip-chip underfill material) so that it would easily fill in the gap between the circuit element (semiconductor substrate) and the circuit board for reinforcement; therefore, it would have been obvious at the time the invention was made to use a liquid underfill encapsulant material in the method of Sakemi, as suggested by Ono et al.

Regarding claim 5, Sakemi is relied upon for the teachings above. Sakemi also teaches that heating the conductive bonding material comprises placing the substrate on a hot plate (8). Sakemi is silent toward heating the substrate to a temperature in a range of approximately 65°C to 85°C.

One skilled in the art would have readily appreciated that the conductive bonding material could be heated in a range of 65°C to 85°C and that the temperature would be dependent on the type of conductive bonding material used; therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to choose a conductive-bonding material that could be heated in the desired range in the method of Sakemi.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of the American Technical Ceramics bulletin, Teshima et al. (6,651,870), Venugopalan et al. (U.S. Pub. 2004/0201110), Hunninghaus et al. (U.S. Patent 5,708,566), and Abramov (U.S. 6,223,419).

Regarding claim 4, Sakemi is relied upon for the teachings above. Sakemi is silent toward the circuit element being one selected from the group containing a capacitor, a resistor, a diode, a transistor, and an inductor.

American Technical Ceramics bulletin, Teshima et al., Venugopalan et al., Hunninghaus et al., and Abramov are all directed toward bonding different circuit elements to circuit boards. The American Technical Ceramics bulletin teaches bonding capacitors to circuit boards (Section 12.0). Teshima et al. teaches bonding resistors to circuit boards (Column 1, lines 14-24; Column 21, lines 55-56). Venugopalan et al. teaches bonding diodes to circuit boards (Abstract; Page 2, paragraph [0021]. Hunninghaus teaches bonding transistors to printed circuit boards (Column 1, lines 18-19; Column 6, lines 60-61). Abramov teaches bonding inductors to printed circuit boards (Column 4, lines 47-51).

One skilled in the art would have readily appreciated using one of the above circuit elements, since they are all conventional items that are bonded to circuit boards; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use one of the above circuit elements in the method of Sakemi, as suggested by the American Technical Ceramics bulletin, Teshima et al., Venugopalan et al., Hunninghaus et al., and Abramov.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable Yagi et al. (U.S. Patent 6,651,320).

Regarding claim 5, Yagi et al. is relied upon for the teaching above. Yagi et al. also teaches that the conductive bonding material can be heated by a heating tool with a heater that heats at least one of the semiconductor element (circuit element) and circuit board. The non-conductive bonding material is heated in a range of 60oC to 200oC, but the conductive material is set in the same process; therefore, it is also heated in the above range. Yagi et al. is silent toward the heating tool being a hot plate.

One skilled in the art would have readily appreciated that the heating tool could be a hot plate, since it is a common object used for heating. One skilled in the art would have also readily recognized that heating in the desired temperature range would depend on the two bonding materials; therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to choose two bonding materials whose desired heating (curing) falls in the above range in the method of Yagi et al.

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of Lane et al. (U.S. Patent 6,599,619).

Regarding claim 8, Sakemi and Ono et al. are relied upon for the teachings above. Sakemi is silent toward the substrate comprising a laminate substrate and the non-conductive bonding material comprising a flip chip underfill material.

The limitations for the non-conductive bonding material comprising a flip chip underfill material are addressed in above in claim 3

Lane et al. is directed toward methods for producing electrical laminates from certain thermosetting resin compositions. Lane et al. teaches that electrical laminates such as circuit boards are produced by laminating sheets of electrical conducting material onto a base substrate of insulation material (Column 1, lines 15-17 and 24-28).

One skilled in the art would have readily appreciated using a laminated substrate, such as a circuit board, since it is a conventional substrate to use when attaching circuit elements; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a laminate substrate in the method of Sakemi, as modified above in claim 3, as suggested by Lane et al.

15. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of Ono et al. (U.S. Patent 6,890,789) and Davis et al. (U.S. Patent 6,590,285).

Regarding claims 9 and 11, Sakemi teaches a method for attaching an electrical device to a circuit board, comprising: applying a conductive adhesive to electrical conductors of at least one of the electrical device and the circuit board, positioning the electrical device relative to the circuit board so that corresponding electrical conductors are aligned and in contact, seating the electrical device in the conductive adhesive, applying an amount of non-conductive bonding material around the edges of the electrical device near the circuit board, and full curing the conductive adhesive and the non-conductive bonding material.

Sakemi is silent toward the gel curing the conductive adhesive at an elevated temperature and that the non-conductive bonding material is a liquid encapsulant material.

Ono et al. is relied upon for the teachings above in claim 3, which includes teaching that the non-conductive bonding material comprises a liquid underfill encapsulant material (flip-chip underfill material) (Figure 8C; Column 10, lines 29-33).

Davis et al. is directed toward a method for mounting an electrical component on a substrate. The method includes applying a conductive adhesive on a contact pad joined to a substrate, aligning a component with the substrate such that at least one lead of the component is juxtaposed with the conductive adhesive, performing a partial (gel) cure of the conductive adhesive, such that an electrical and mechanical connection suitable for testing is formed, testing performance of the component, and performing a full cure of the conductive adhesive such that a permanent connection is formed (Column 2, lines 51-67). Davis et al. teaches gel curing the conductive adhesive at an elevated temperature (Column 5, lines 35-42).

One skilled in the art would have readily appreciated that the non-conductive bonding material is a liquid underfill encapsulant material (flip-chip underfill material) so that it easily fills in the gap between the circuit element (semiconductor substrate) and the circuit board for reinforcement in the process of Ono et al. Also one skilled in the art would have readily appreciated gel curing the conductive adhesive before the full cure to allow for adjustments of misaligned components in the process of Davis et al. (Column 2, lines 64-67). Therefore, it would have been obvious to one of ordinary skill

in the art at the time the invention was made to uses liquid underfill encapsulant material and to gel cure the conductive adhesive before the full cure in the method of Sakemi as suggested by Ono et al. and Davis et al.

Applicant also added the new limitation of the liquid encapsulant material being applied around only the edge of an area where the electrical device overlies the circuit board. Sakemi teaches this limitation in Figure 1C.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of Ono et al. (U.S. Patent 6,890,789) and Davis et al. (U.S. Patent 6,590,285), as applied to claims 9 and 11, and further in view of the American Technical Ceramics bulletin, Teshima et al. (6,651,870), Venugopalan et al. (U.S. Pub. 2004/0201110), Hunninghaus et al. (U.S. Patent 5,708,566), and Abramov (U.S. 6,223,419).

Regarding claim 10, Sakemi, Ono et al., and Davis et al. are relied upon for the teachings above. Sakemi is silent toward the electrical device being one selected from the group containing a capacitor, a resistor, a diode, a transistor, and an inductor.

American Technical Ceramics bulletin, Teshima et al., Venugopalan et al., Hunninghaus et al., and Abramov are all directed toward bonding different circuit elements to circuit boards. The American Technical Ceramics bulletin teaches bonding capacitors to circuit boards (Section 12.0). Teshima et al. teaches bonding resistors to circuit boards (Column 1, lines 14-24; Column 21, lines 55-56). Venugopalan et al. teaches bonding diodes to circuit boards (Abstract; Page 2, paragraph [0021].

Hunninghaus teaches bonding transistors to printed circuit boards (Column 1, lines 18-19; Column 6, lines 60-61). Abramov teaches bonding inductors to printed circuit boards (Column 4, lines 47-51).

One skilled in the art would have readily appreciated using one of the above electrical devices, since they are all conventional items that are bonded to circuit boards; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use one of the above electrical devices in the method of Sakemi, as modified above, as suggested by the American Technical Ceramics bulletin, Teshima et al., Venugopalan et al., Hunninghaus et al., and Abramov.

17. Claims 12 and13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of Ono et al. (U.S. Patent 6,890,789) and Davis et al. (U.S. Patent 6,590,285), as applied to claims 9 and 11, and further in view of the American Technical Ceramics bulletin.

Regarding claims 12 and 13, Sakemi, Ono et al., Davis et al., and the American Technical Ceramics bulletin are relied upon for the teachings above. Sakemi is silent toward the conductive adhesive comprising of a silver epoxy resin or a gold epoxy resin.

The American Technical Ceramics bulletin teaches that there are essentially two choices in conductive epoxies for capacitor chip attachment: silver epoxy and gold epoxy (Section 12.0).

One skilled in the art would have readily appreciated using one of the conventional conductive epoxies (silver or gold) to bond an electrical device to a circuit

board, and the choice should be dependent on material compatibility (gold conductors bonded with gold epoxy and silver conductors bonded with silver epoxy). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a gold or silver epoxy as the conductive adhesive in the method of Sakemi, as modified above, as suggested by the American Technical Ceramics bulletin.

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakemi (U.S. Patent 5,817,542) in view of Ono et al. (U.S. Patent 6,890,789) and Davis et al. (U.S. Patent 6,590,285), as applied to claims 9 and 11, and further in view of Lane et al. (U.S. Patent 6,599,619).

Regarding claim 8, Sakemi, Ono et al., and Davis et al. are relied upon for the teachings above. Sakemi is silent toward the circuit board comprising a laminate substrate.

Lane et al. is directed toward methods for producing electrical laminates from certain thermosetting resin compositions. Lane et al. teaches that electrical laminates such as circuit boards are produced by laminating sheets of electrical conducting material onto a base substrate of insulation material (Column 1, lines 15-17 and 24-28).

One skilled in the art would have readily appreciated using a circuit board that comprises a laminate substrate, since it is a conventional substrate to use when attaching electrical devices; therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a circuit board that comprises a

laminate substrate in the method of Sakemi, as modified above, as suggested by Lane et al.

Response to Arguments

19. Applicant's arguments filed 11/4/05 have been fully considered but they are not persuasive. Applicant argued that the Sakemi and Yagi et al. references do not teach the added limitation of the non-conductive bonding material being applied around only the edge of an area. The limitation is new matter and it is unclear where this edge area is and what the edge of an area entails as discussed in paragraphs 2 and 4 above. Therefore, taking the broadest possible meaning of "the edge of an area", the Sakemi and Yagi references teach this limitation in that they show applying the non-conducting bonding material from outside of the circuit element.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jayme L. Brown** whose telephone number is **571-272-8386**. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 571-272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jayme L. Brown

GLADYS J.P. CORCORAN
PRIMARY EXAMINER